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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,083	10/21/2003	Kesami Hagiwara	XA-9954	1915

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MCLEAN, VA 22102-3833

EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,083	HAGIWARA ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *21 October 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Preliminary Amendment and IDS as received on 10/21/2003, and Foreign Priority Papers as received on 3/19/2004.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 5 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Regarding claims 5 and 8, the phrase "such as" renders the claims indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-9, 11, and 13-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Mitsuishi, U.S. Patent No. 6,745,320.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

9. Referring to claim 1, Mitsuishi has taught a data processor comprising:

a) n-bit instructions and 2n-bit instructions in an instruction set. See Fig.9, and note instruction format (2), which corresponds to an n-bit instruction, and instruction format (4), which corresponds to 2n-bit instructions.

b) wherein the 2n-bit instructions including register specification fields include the register specification fields in the first half n bits thereof. See Fig.9, format (4). Note that r1 and r2 are in the first half of the instruction.

c) wherein the register specification fields in the first half n bits have the same placement as register specification fields in the n-bit instructions. See Fig.9 and note that formats (2) and (4) have the same placement of registers (i.e., after the opcode).

d) while Mitsuishi has not explicitly taught an instruction control unit that can decide whether registers specified in register specification fields of the instructions conflict between the instructions, the examiner deems this limitation to be inherent. For proper execution, register conflict issues (dependencies) must be identified and resolved. Failure to resolve these issues would result in instructions executing based on incorrect data, which would yield an overall incorrect result. This is clearly undesirable. Therefore, a unit must detect register conflicts between instructions.

10. Referring to claim 2, Mitsuishi has taught a data processor comprising:

a) n-bit instructions and 2n-bit instructions in an instruction set. See Fig.9, and note instruction format (2), which corresponds to an n-bit instruction, and instruction format (4), which corresponds to 2n-bit instructions.

b) wherein the 2n-bit instructions including register specification fields include the register specification fields in one of the first half n bits or latter half n bits thereof. See Fig.9, format (4). Note that r1 and r2 are in the first half of the instruction.

c) wherein the register specification fields in the first half n bits or latter half n bits include the same placement as register specification fields in the n-bit instructions. See Fig.9 and note that formats (2) and (4) have the same placement of registers (i.e., after the opcode).

d) while Mitsuishi has not explicitly taught an instruction control unit that can decide whether registers specified in register specification fields of the instructions conflict between the

instructions, the examiner deems this limitation to be inherent. For proper execution, register conflict issues (dependencies) must be identified and resolved. Failure to resolve these issues would result in instructions executing based on incorrect data, which would yield an overall incorrect result. This is clearly undesirable. Therefore, a unit must detect register conflicts between instructions.

11. Referring to claim 3, Mitsuishi has taught a data processor as described in claim 2. Mitsuishi has further taught that:

a) the instruction set comprises instructions in which register specification fields aligned with the register specification fields in the n-bit instructions are placed in the first half n bits of the 2n-bit instructions. See Fig.9. Note that instruction format (2) corresponds to original n-bit instructions while instruction format (4) corresponds to 2n-bit instructions having register specifiers in the first half.

b) wherein the instruction set further comprises instructions in which register specification fields aligned with the register specification fields in the n-bit instructions are placed in the latter half n bits of the 2n-bit instructions. See Fig.9, and column 40, lines 6-15. Note that instruction format (2) corresponds to original n-bit instructions while instruction format (3) corresponds to 2n-bit instructions having register specifiers in the second half.

12. Referring to claim 4, Mitsuishi has taught a data processor as described in claim 1. Mitsuishi has further taught that n bits are 16 bits and 2n bits are 32 bits. See column 2, lines 23-24, and note that a basic instruction, such as the one shown in Fig.9 (format (2)) is 16 bits. Then, formats (3) and (4) are clearly double the size of format (2), making them 32 bits.

13. Referring to claim 5, Mitsuishi has taught a data processor as described in claim 1. While Mitsuishi has not explicitly taught that the instruction control unit, in response to register conflict, is able to perform control such as the stalling of pipeline stages or the forwarding of operation data write to general purpose registers, the examiner deems this limitation to be inherent. Specifically, if forwarding hardware does not exist in Mitsuishi, then stalling must exist to resolve register conflicts, as there is no other way to prevent a consumer instruction from using a non-ready value.

14. Referring to claim 6, Mitsuishi has taught a data processor as described in claim 1. Mitsuishi has further taught that the data processor is able to execute instructions in single scalar mode. From column 96, line 65, to column 97, line 6, it is disclosed that operations may be executed in parallel by more than one execution unit. Consequently, the processor is superscalar in nature. However, if a processor is able to execute multiple operations at a time, then it is also able to execute one operation at a time (single scalar mode).

15. Referring to claim 7, Mitsuishi has taught a data processor as described in claim 1. Mitsuishi has further taught that the data processor can execute instructions in superscalar mode. See column 96, line 65, to column 97, line 6, and note that it is disclosed that operations may be executed in parallel by more than one execution unit. Consequently, the processor is superscalar in nature.

16. Referring to claim 8, Mitsuishi has taught a data processor as described in claim 2. While Mitsuishi has not explicitly taught that the instruction control unit, in response to register conflict, is able to perform control such as the stalling of pipeline stages or the forwarding of operation data write to general purpose registers, the examiner deems this limitation to be

inherent. Specifically, if forwarding hardware does not exist in Mitsuishi, then stalling must exist to resolve register conflicts, as there is no other way to prevent a consumer instruction from using a non-ready value.

17. Referring to claim 9, Mitsuishi has taught a data processor comprising:

a) first n-bit instructions and second 2n-bit instructions each including register specification fields in an instruction set. See Fig.10, and note instruction format (1), which corresponds to an n-bit instruction, and instruction format (3), which corresponds to 2n-bit instructions.

b) wherein the second instructions are instructions with an immediate value or displacement value extended to the first instructions. See Fig.10, format (3).

c) wherein the second instructions include register specification fields in the first half n bits thereof. See Fig.10, format (3).

d) wherein the register specification fields in the first half n bits of the second instruction comprises the same placement as the register specification fields in the first instructions. See Fig.10, formats (1) and (3).

18. Referring to claim 11, Mitsuishi has taught a data processor comprising:

a) first n-bit instructions and second 2n-bit instructions each including register specification fields in an instruction set. See Fig.9, and note instruction format (2), which corresponds to an n-bit instruction, and instruction formats (3) and (4), which correspond to 2n-bit instructions.

b) wherein the second instructions include register specification fields in one of the first half n bits and the latter half n bits thereof. See Fig.9, format (4). Note that r1 and r2 are in the first half of the instruction. Alternatively, format (3) has register fields in the latter half of the instruction.

c) wherein the placement of the register specification fields in the first half n bits or the latter half n bits is the same as the placement of the register specification fields in the first instructions. See Fig.9 and note that formats (2) and (4) have the same placement of registers (i.e., after the opcode). Formats (2) and (3) also have aligned register fields.

19. Referring to claim 13, Mitsuishi has taught a data processor as described in claim 2. Furthermore, claim 13 is rejected for the same reasons set forth in the rejection of claim 6.

20. Referring to claim 14, Mitsuishi has taught a data processor as described in claim 3. Furthermore, claim 14 is rejected for the same reasons set forth in the rejection of claim 7.

21. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

22. Claims 9 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Watanabe, U.S. Patent No. 4,710,867.

23. Referring to claim 9, Watanabe has taught a data processor comprising:

a) first n-bit instructions and second 2n-bit instructions each including register specification fields in an instruction set. See Fig.2A and Fig.2B.

b) wherein the second instructions are instructions with an immediate value or displacement value extended to the first instructions. See Fig.2B and column 3, lines 16-20.

c) wherein the second instructions include register specification fields in the first half n bits thereof. See Fig.2B (note all register specifiers (Rx, Ry, and Rz) are in the first half of the instruction).

d) wherein the register specification fields in the first half n bits of the second instruction comprises the same placement as the register specification fields in the first instructions. See Fig.2A and Fig.2B.

24. Referring to claim 11, Watanabe has taught a data processor comprising:

a) first n-bit instructions and second 2n-bit instructions each including register specification fields in an instruction set. See Fig.2A and Fig.2B.

b) wherein the second instructions include register specification fields in one of the first half n bits and the latter half n bits thereof. See Fig.2B (note all register specifiers (Rx, Ry, and Rz) are in the first half of the instruction).

c) wherein the placement of the register specification fields in the first half n bits or the latter half n bits is the same as the placement of the register specification fields in the first instructions. See Fig.2A and Fig.2B.

25. Claims 9-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshida, U.S. Patent No. 5,761,470.

26. Referring to claim 9, Yoshida has taught a data processor comprising:

a) first n-bit instructions and second 2n-bit instructions each including register specification fields in an instruction set. See Fig.3 (SR) and Fig.4 (LM-1).

b) wherein the second instructions are instructions with an immediate value or displacement value extended to the first instructions. See Fig.4 (LM-1).

c) wherein the second instructions include register specification fields in the first half n bits thereof. See Fig.4 (LM-1).

d) wherein the register specification fields in the first half n bits of the second instruction comprises the same placement as the register specification fields in the first instructions. See Fig.3 (SR) and Fig.4 (LM-1).

27. Referring to claim 10, Yoshida has taught a data processor as described in claim 9. Yoshida has further taught that the data processor includes:

a) third n-bit instructions including register specification fields. See Fig.4 (LR-R).

b) wherein the third instructions and the second instructions are different from each other in the number of operands specifiable in the register specification fields. See Fig.4 and note that LR-R specifies at least 4 registers (Ra-Rd) while LM-1 specifies 2 registers (Ra, Rb).

c) wherein register specification fields of the third instructions and those of the second instructions are aligned in the start of the register specification fields with respect to the start of the first instructions. See Fig.3 (SR) and Fig.4 (PM-1 and LR-R) and note that each of the Ra's and Rb's are aligned.

28. Referring to claim 11, Watanabe has taught a data processor comprising:

a) first n-bit instructions and second 2n-bit instructions each including register specification fields in an instruction set. See Fig.3 (SR) and Fig.4 (LM-1).

b) wherein the second instructions include register specification fields in one of the first half n bits and the latter half n bits thereof. See Fig.4 (LM-1).

c) wherein the placement of the register specification fields in the first half n bits or the latter half n bits is the same as the placement of the register specification fields in the first instructions. See Fig.3 (SR) and Fig.4 (LM-1).

29. Referring to claim 12, Yoshida has taught a data processor as described in claim 11. Furthermore, claim 12 is rejected for the same reasons set forth in the rejection of claim 10.

Claim Rejections - 35 USC § 103

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

31. Claims 1-2, 4-8, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe.

32. Referring to claim 1, Watanabe has taught a data processor comprising:

a) n-bit instructions and 2n-bit instructions in an instruction set. See Fig.2A and Fig.2B.

b) wherein the 2n-bit instructions including register specification fields include the register specification fields in the first half n bits thereof. See Fig.2B (note all register specifiers (Rx, Ry, and Rz) are in the first half of the instruction).

c) wherein the register specification fields in the first half n bits have the same placement as register specification fields in the n-bit instructions. See Fig.2A and Fig.2B.

d) Watanabe has not explicitly taught an instruction control unit that can decide whether registers specified in register specification fields of the instructions conflict between the instructions.

However, Official Notice is taken that detecting register conflict (i.e., dependencies) and its advantages are well known and accepted in the art. Specifically, it is well known that a consumer instruction needs to use the result written to a register by a previous instruction (producer instruction). It is also known that sometimes the result of the producer instruction is unavailable when the consumer instruction first needs it. For instance, a common hazard is a RAW hazard, which occurs when a consumer instruction tries to read a register before the producer instruction writes its result to that register. Consequently, appropriate action must be taken so that the consumer does not read an incorrect register value. If appropriate action is not taken, then incorrect results would be achieved, and this is clearly undesirable. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Watanabe such that register conflict is detected between the instructions shown in Fig.2A and Fig.2B. Such a modification would ensure that correct execution is achieved.

33. Referring to claim 2, Watanabe has taught a data processor comprising:

a) n-bit instructions and 2n-bit instructions in an instruction set. See Fig.2A and Fig.2B.

b) wherein the 2n-bit instructions including register specification fields include the register specification fields in one of the first half n bits or latter half n bits thereof. See Fig.2B (note all register specifiers (Rx, Ry, and Rz) are in the first half of the instruction).

c) wherein the register specification fields in the first half n bits or latter half n bits include the same placement as register specification fields in the n-bit instructions. See Fig.2A and Fig.2B.

d) Watanabe has not explicitly taught an instruction control unit that can decide whether registers specified in register specification fields of the instructions conflict between the instructions. However, Official Notice is taken that detecting register conflict (i.e., dependencies) and its

advantages are well known and accepted in the art. Specifically, it is well known that a consumer instruction needs to use the result written to a register by a previous instruction (producer instruction). It is also known that sometimes the result of the producer instruction is unavailable when the consumer instruction first needs it. For instance, a common hazard is a RAW hazard, which occurs when a consumer instruction tries to read a register before the producer instruction writes its result to that register. Consequently, appropriate action must be taken so that the consumer does not read an incorrect register value. If appropriate action is not taken, then incorrect results would be achieved, and this is clearly undesirable. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Watanabe such that register conflict is detected between the instructions shown in Fig.2A and Fig.2B. Such a modification would ensure that correct execution is achieved.

34. Referring to claim 4, Watanabe has taught a data processor as described in claim 1. Watanabe has taught that n bits are 32 bits and 2n bits are 64 bits (Fig.2A-B) but has not taught that n bits are 16 bits and 2n bits are 32 bits. However, Official Notice is taken that instruction sizes of 8, 16, 32, and 64 bits are well known in the art and the sizes chosen are as a result of design choice. As the bit sizes increase, more information can be stored in an instruction, allowing for more opcodes (more overall instructions), more registers, larger immediate values, etc. However, as the bit sizes increase, the memory required to store those instructions increase. Sizes of 16 and 32 bits fall in the middle where a good amount of information may be encoded while not requiring as much store as 64-bit instructions (which would require double the storage that 32-bit instructions require). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Watanabe such that the instructions are 16 and 32

bits, respectively. Furthermore, as shown in In re Rose, 105 USPQ 237 (CCPA 1955), changes in size/range are generally not given patentable weight or would have been obvious improvements.

35. Referring to claim 5, Watanabe has taught a data processor as described in claim 1. Watanabe has not taught that the instruction control unit, in response to register conflict, is able to perform control such as the stalling of pipeline stages or the forwarding of operation data write to general purpose registers, the examiner deems this limitation to be inherent. However, Official Notice is taken that stalling and forwarding are known ways of resolving register conflicts. Forwarding hardware allows the result of a producer instruction to be passed to a consumer instruction before it is written to the register file. This allows the consumer to refrain from stalling since the data is available sooner. As a result, in order to prevent stalling, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Watanabe to perform forwarding.

36. Referring to claim 6, Watanabe has taught a data processor as described in claim 1. Watanabe has further taught that the data processor is able to execute instructions in single scalar mode. From Fig.1, it can be seen that multiple execution units (510-513) exist which work together to execute multiple instructions at once. Consequently, the processor is superscalar in nature. However, if a processor is able to execute multiple operations at a time, then it is also able to execute one operation at a time (single scalar mode).

37. Referring to claim 7, Watanabe has taught a data processor as described in claim 1. Watanabe has further taught that the data processor can execute instructions in superscalar mode.

See Fig.1 and note that multiple operations may be executed in parallel by more than one execution unit. Consequently, the processor is superscalar in nature.

38. Referring to claim 8, Watanabe has taught a data processor as described in claim 2. While Watanabe has not explicitly taught that the instruction control unit, in response to register conflict, is able to perform control such as the stalling of pipeline stages or the forwarding of operation data write to general purpose registers, the examiner deems this limitation to be inherent. Specifically, if forwarding hardware does not exist in Mitsuishi, then stalling must exist to resolve register conflicts, as there is no other way to prevent a consumer instruction from using a non-ready value.

39. Referring to claim 13, Watanabe has taught a data processor as described in claim 2. Furthermore, claim 13 is rejected for the same reasons set forth in the rejection of claim 6.

40. Claims 10 and 12 are rejected under 35 U.S.C. 103(a) as being obvious over Mitsuishi. The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in

the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

41. Referring to claim 10, Mitsuishi has taught a data processor as described in claim 9. Mitsuishi has not explicitly taught that the data processor includes third n-bit instructions including register specification fields, wherein the third instructions and the second instructions are different from each other in the number of operands specifiable in the register specification fields, and wherein register specification fields of the third instructions and those of the second instructions are aligned in the start of the register specification fields with respect to the start of the first instructions. However, it should be realized that the first instructions may be considered the add.w instructions shown as an example in Fig.9 under format (2). Official Notice is taken that there are other well known operations such as subtract, multiply, and divide, which would also fit this format. Adding any or all of the instructions would increase the functionality of the processor and therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have third n-bit instructions to be sub.w instructions, for instance. Then, it can be seen that the sub.w instructions would have aligned registers with the first and second instructions (i.e., after the opcode). And, it can be seen that the sub.w instruction's r1 field is larger than that of format (4), which means that it may specify more registers.

42. Referring to claim 12, Mitsuishi has taught a data processor as described in claim 11. Furthermore, claim 12 is rejected for the same reasons set forth in the rejection of claim 10.

Conclusion

43. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Itomitsu et al., U.S. Patent No. 4,945,511, has taught an improved pipelined processor with two stage decoder for exchanging register values for similar operand instructions in which instructions are extended.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJH
David J. Huisman
June 6, 2006

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SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100